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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,129	03/06/2002	Wolfgang Ernst	1406/48	8745

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JENKINS & WILSON, PA
3100 TOWER BLVD
SUITE 1400
DURHAM, NC 27707

EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,129	ERNST ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *30062000*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 have been examined.

Claim Objections

2. Claim 1 is objected to because of the following informalities: In all occurrences of the limitation "which, in a manner dependent" should read "which, in a manner is dependent". Appropriate correction is required.

3. Claim 1 is objected to because of the following informalities: The number (61) should be removed from the claim language as indicated from the amended claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1:

This claim recites the limitation "the through-connected base address register" on line 13 and "the through-connected base offset register" on line 16. There is insufficient antecedent basis for this limitation in the claim.

Claims 2-10:

These claims are also rejected because they depend on claim 1 and have the same problems of insufficient antecedent basis.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yazawa (US-5657466) herinafter Yazawa, in view of Tanaka et al. (US-4779084), hereinafter Tanaka, in further view of Eastburn (US-5883905).

Claim 1:

Yazawa teaches an address generation circuit comprising a pointer register 1 (base address register), a write offset register set 7, a read offset register set 8 (offset registers), a multiplexer 3, and an adder 4 (addition circuit). Yazawa teaches the write and read offset register sets 7 and 8 respectively have a plurality of offset registers having different offset values corresponding to the required delay amount. Yazawa also teaches the multiplexer 3 selects a register of the write and read offset register sets 7 and 8, respectively, based on a read/write (abbreviated RD/WR hereinafter) control signal (offset register selection control signal). The adder 4, coupled to the pointer register 1 and the multiplexer 3, adds the output of the pointer register 1 to that of the

multiplexer 3 to generate a write or read address. (Col. 3, lines 21-38, Fig. 2). Yazawa does not explicitly teach the pointer register 1 (base address register) switching through a first multiplexer to a first input of an addition unit. However, Yazawa does teach that adder 4 is coupled to the pointer register. Tanaka teaches a start address register 14 (base address register), connected to bus 2, is coupled to selector 15 (first multiplexer circuit), which output data from the start address register 14. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yazawa's pointer register 1 (base address register) to incorporate Tanaka's start address register 14 and selector 15 (first multiplexer circuit). The artisan would have been motivated to do so because this would afford Yazawa the flexibility to select between the two registers for address and offset value selection. The artisan would have been motivated to do so because now Yazawa would be able to add the address from the output of Tanaka's selector 15 (first multiplexer circuit) with the output of the multiplexer 3 (offset address). Yazawa does not explicitly teach a second mutiplexer, which connects the offset register group to a third multiplexer, which then connects to the second input of the addition circuit. However, Yazawa does teach the adder 4 (addition circuit), coupled to the pointer register 1 (base address register, now modified by Tanaka's start address register 14 and selector 15 (first multiplexer circuit)) and the multiplexer 3, adds the output of the pointer register 1 to that of the multiplexer 3 to generate a write or read address. Eastburn teaches the address scrambler 200 combines a crosspoint multiplexer 201 (second multiplexer) and a pair of scramble memories (XSCRM and YSCRM) 202 and 204, which are initialized (programmed) at

APG setup time. Eastburn teaches the multiplexer 201 receives X, Y, and Z addresses from the X, Y, and Z ALUs (offset register group). Eastburn suggests the scramble memories may be bypassed altogether by use of bypass multiplexer (not shown). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yazawa's address generation circuit by adding Eastburn's crosspoint multiplexer 201 (second multiplexer) to connect to Yazawa's offset registers 7 and 8. The artisan would have been motivated to do so because this would enable Yazawa to create a multidimensional address. The artisan would have been motivated to do so because now Yazawa can select between the offset registers 7 and 8 through Eastburn's crosspoint multiplexer 201 (second multiplexer) with multiplexer 3 (third multiplexer) and convey this selected offset address to adder 4 being controlled by the read/write (abbreviated RD/WR hereinafter) control signal (offset register selection control signal).

Claim 2:

Tanaka teaches the offset value is set into the offset register 13 (both programmable and fixed) and the start address is changed from A1 to A2 in accordance with an instruction via the bus 2 from the CPU1 (external test device). (See col. 3, lines 10-12, 30-31).

Claim 3:

Eastburn teaches gate 223 inverts the invert value or not according to the state of the latched inversion register 222 (controllable inverting circuit), which allows for easy

programming of a pattern and its inverse with the insertion of a single pattern instruction to change the state of the latch inversion register 222. (Col. 7, lines 18-30).

Claim 4:

Yazawa teaches when the RD control signal (RD/WR=1) is supplied to the multiplexer 3, the address generation circuit generates the read address. That is, one of the offset registers in the read offset register set 8 is selected to provide one of offset values A, B, C and D stored therein (the number of offset registers is equal to the number of the address test jump variants). (Col. 3, lines 49-53).

Claim 5:

Yazawa teaches the present invention relates to a circuit for generating an address of a RAM (SRAM). Col. 1, lines 11-13).

Claim 6:

Yazawa teaches the present invention relates to a circuit for generating an address of a RAM (SRAM). Col. 1, lines 11-13). It is commonly known to those skilled in the art that RAMs have a multiplicity of memory cells which can be addressed via a multidimensional address space.

Claim 7:

Yazawa teaches the adder 4 adds the selected offset value to the pointer value from the pointer register 1 (base address registers) so as to generate the write address WAD. (Col. 3, lines 46-48). Yazawa does not explicitly disclose the number of base address registers. In light of the modification to combine Yazawa with Tanaka, it would have been obvious to one of ordinary skill in the art at the time the invention was made

that Yazawa would have the number of the pointer register 1 (base address registers) correspond to the number of addresses needed (dimension of the address space). The artisan would have been motivated to do so because it would enable Yazawa to address a wide range of memories with varying memory address space.

Claim 8:

Yazawa teaches the RD/WR control signal (offset register selection control signal) which controls multiplexer 3 (third multiplexer) is controlled by the control unit (not shown). (Col. 3, lines21-35). Tanaka teaches the offset value is set into the offset register 13 (both programmable and fixed) and the start address is changed from A1 to A2 in accordance with an instruction via the bus 2 from the CPU1 (external test device). (See col. 3, lines 10-12, 30-31).

Claim 9:

Yazawa illustrates all the limitations in Figure 2.

Claim 10:

Yazawa teaches the present invention relates to a circuit for generating an address of a RAM (integrated in the circuit to be tested). Col. 1, lines 11-15).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133